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(54) Multi-layer ceramic package for semiconductor chip

(57) In a multi-layer ceramic package wherein a plurality of ceramic laminates each has a conductive pattern, and wherein there is an internal cavity of the package within which is bonded a chip or a plurality of chips interconnected to form a chip array, the chip or chip array (16) is connected through short wire bonds (42) at varying laminate levels each having metalized conductive patterns thereon, and the conductive patterns on the respective laminate layers are interconnected either by tunnel openings (32) filled with metalized material, or by edge formed metalizations (34) so that the conductive patterns ultimately connect to a number of pads at the undersurface of the ceramic package when mounted on to a metalized board. There is achieved a high component density, but because the connecting wire leads are "staggered" or connected at alternating points at package levels, it is possible to maintain a 10 mil spacing and 10 mil size of the wire bond lands.

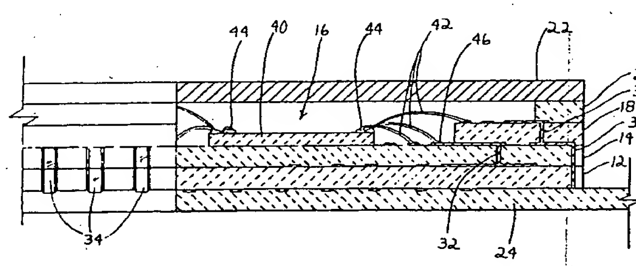

FIG. 3

GB 2 077 036 A

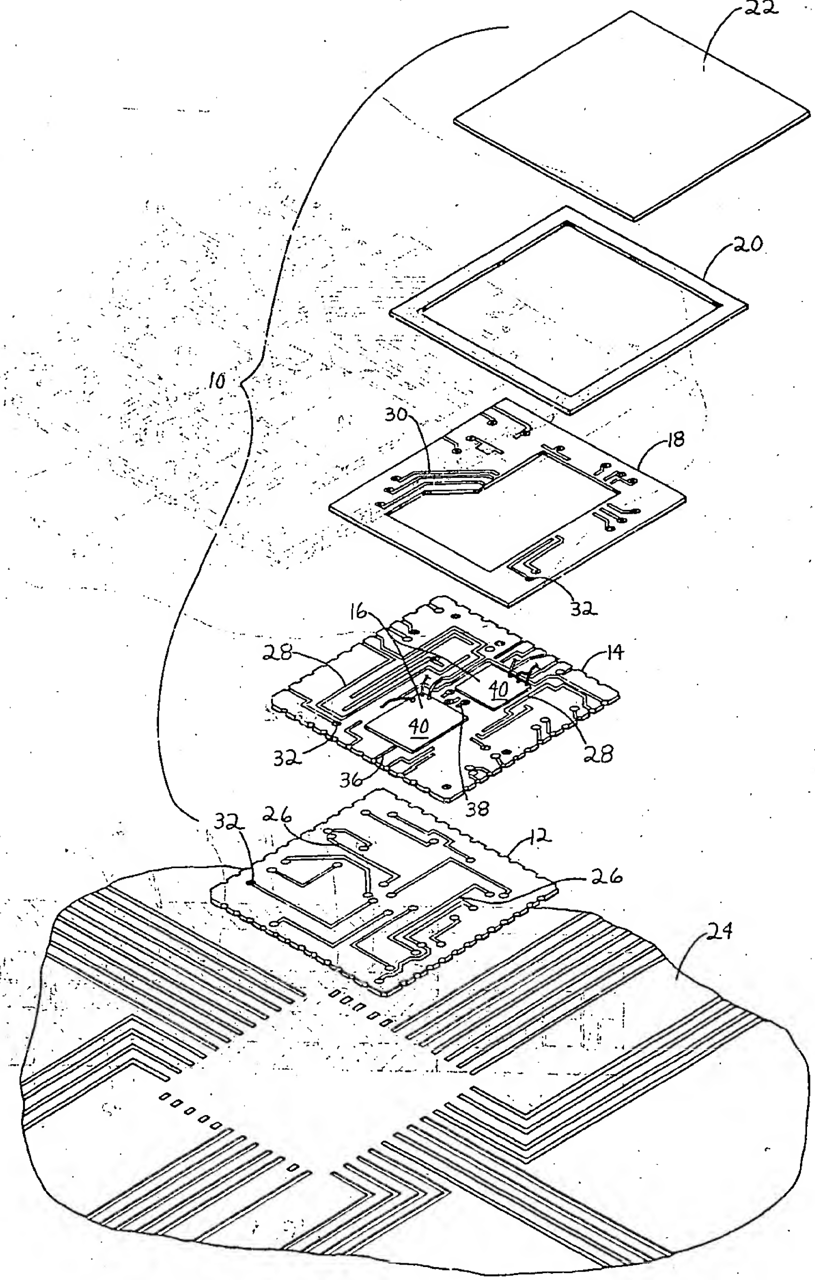

FIG. 1

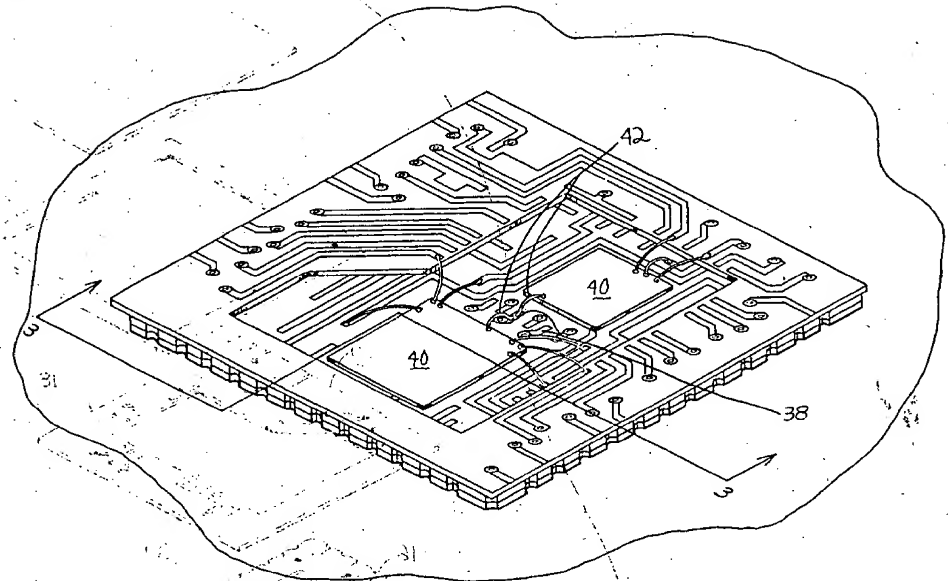

FIG. 2

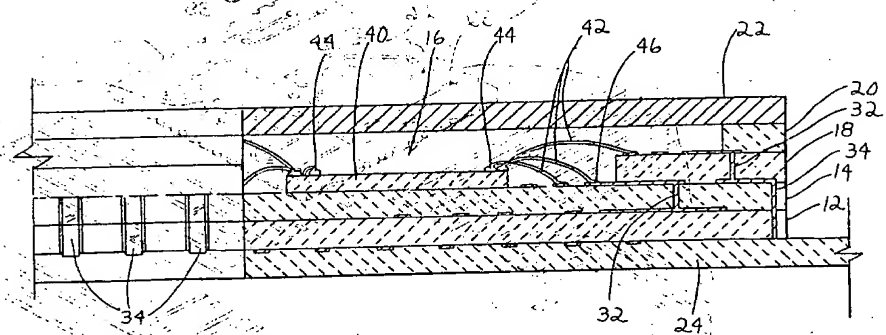

FIG. 3

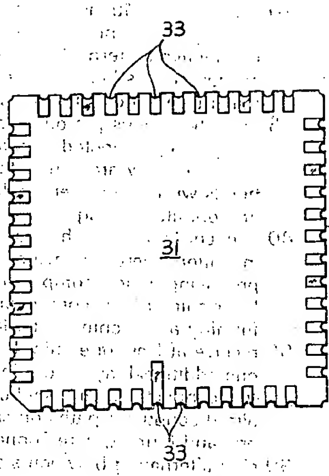

FIG. 4

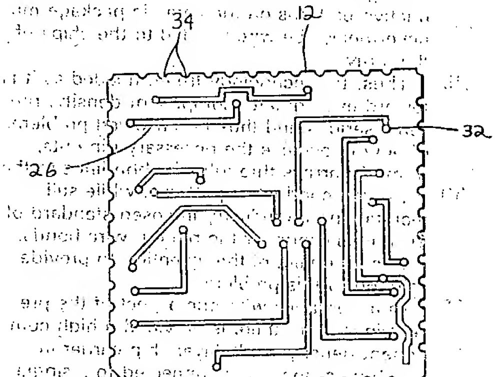

FIG. 4a

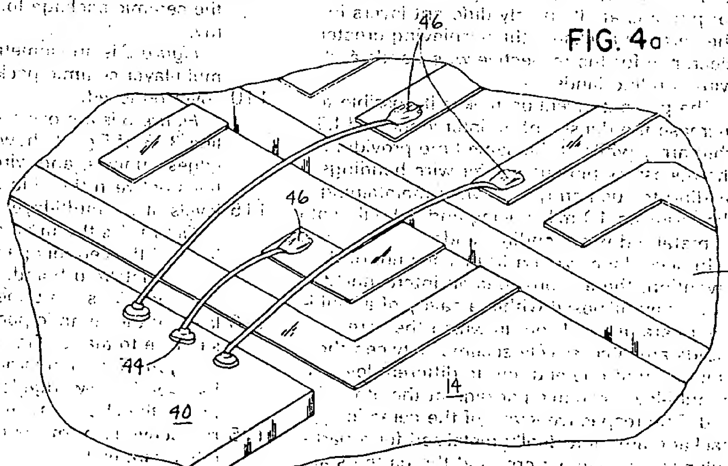

FIG. 5

SPECIFICATION

Multi-layer ceramic package

In the packaging of interconnected chip or chip arrays, wire bondings from the chip or chip array, particularly where there is a high component density, or where bonding pads on chips are closely spaced, are excessively crowded, so that there is a real danger that the wire bonds will come into too close proximity with each other and present a serious difficulty in maintaining required spacing for the wires and the bonding lands. This is because the conductive patterns converge upon the chips from the printed metalized patterns provided on the single ceramic laminate. The result is overcrowding of the wire conductors or bondings. However, the trend in multiple circuit chip structures is toward even greater component density, and the conductive patterns on the ceramic package must nevertheless be wire bonded to the chips of the array.

Thus, the technology trend, headed as it is toward even greater component density, presents serious and thus far unsolved problems of how to achieve the necessary pin outs, from LSI arrays through wire bondings to the metalized conductive patterns, while still maintaining an industry imposed standard of 10 mil spacings for the pin out wire bonds.

It is an object of the invention to provide a solution to this problem.

In accordance with one aspect of the present invention, there is provided a high component density, multi-layer chip carrier in which wire bonds are connected to a single chip or to chips interconnected in a chip array, with the wire bondings then disposed for pin-outs at alternately different layers in the ceramic package, thus achieving greater clearance for the respective wire bonds and wire bonding lands.

The present invention makes it possible to increase the density of an interconnected LSI chip array while at the same time providing the necessary pin outputs for wire bondings leading to such array and while maintaining the requisite 10 mil spacing and 10 mil width of metalized wire bonding lands.

In accordance with a further feature of the invention, there is provided an interconnected chip array disposed within a cavity of a multi-layer ceramic package, in which the wire bonds are successively secured between the chip array at one end and to different levels of a multi-layer ceramic package at the other end. The respective levels of the ceramic package are individually metalized for a particular conductive pattern, and the patterns are connected through either or both of metalized connections in the form of "tunneled through" openings from one layer to the other edge metalizations so that the respective conductive patterns are connected, leading ultimately to a series of pads at the undersurface of the ceramic package.

Generally, therefore, the present invention provides a multi-layer ceramic package having various level laminates each with a particular conductive pattern, the patterns on the respective layers being connected by either tunneled through or edge metalization bonding, or both. Various pin outs from a central disposed interconnected chip array, disposed within a cavity are connected through wire bonds with said patterns while maintaining an appropriate spacing one relative to the other.

According to another aspect of the present invention, there is provided a method for producing a high component density multi-layer chip carrier, comprising the steps of forming a first chip carrier layer adapted to receive at least one chip thereon, and at least one additional layer, forming pin-out conductive connections with said chip, forming metalized conductor paths on said respective layers, and forming wire connections from said chip alternating between staggered paths respectively formed on the differing levels of said layers.

Further features of the present invention will become apparent from a consideration of the following description which proceeds with reference to the accompanying drawings in which selected example embodiments are illustrated by way of example and not by way of limitation.

In the accompanying drawings:—

Figure 1 is an isometric exploded view illustrating a multi-layer ceramic package, with a printed circuit board at the lower portion and a combination ring and cover at the upper portion which seals an internal cavity in the ceramic package for receiving a chip array;

Figure 2 is an isometric detail view of a multi-layer ceramic package with the ring and cover removed;

Figure 3 is a cross sectional view taken on line 3—3 of Fig. 2 showing the metalized edges, tunnels, and wire bond-pattern connections between the chip array and the various levels of the multi-layer ceramic package;

Figure 4 is the undersurface of the base layer of the ceramic package to be mounted to the metalized board;

Figure 4A is the upper surface of the base layer of the ceramic package and is the opposite face to that of Fig. 4; and

Figure 5 is an enlarged detail view of the ball bond and wedge leads of the wire between the chip array at one wire end and a respective layer of the ceramic package at the other wire end.

Referring to Fig. 1, a multi-layer ceramic package designated generally by reference numeral 10 includes multi-layers of ceramic substrate including a base layer 12, intermediate

layer 14 on which is mounted an interconnected chip array 16, an upper frame layer 18, a ring layer 20, and a cover layer 22. The multi-layer ceramic package as a whole is mounted on a metalized board 24.

The base layer 12, intermediate layer 14, and frame layer 18 each has a printed conductive pattern illustrated by reference numeral 26 in the base layer 12, by reference numeral 28 in the intermediate layer, and by reference numeral 30 for the frame layer 18. The particular pattern of these conductive metalization paths is not a part of the present invention. However, it is contemplated that, prior to assembly, the "green" or unfused ceramic substrates have formed thereon the conductive patterns which are then matched together and electrically connected through connections leading ultimately to pads 33 on the undersurface 31 (Fig. 4) of the base layer 12 for the metalized board 24.

The conductive patterns are communicated one layer with the next, in one instance through "tunnels" 32 (Fig. 3) which are in the form of vertical through openings filled with metalization, and which connect the conductive patterns of one layer to the next. In another instance the conductive patterns of the respective laminates are connected through edge metalizations 34 (Fig. 3).

The interconnected chip array 16 consists of component LSI chips which are connected together. The chips are connected by metalization printed circuits constructed on the confronting surface of intermediate layer 14, and indicated by reference numeral 36.

Between the chips, and to obviate the necessity for the wire bondings to be connected from a chip first outwardly to the periphery of the package and then back to another chip, there can be chip-to-chip wire bonding through lands 38 disposed between and separating the chips 40. These wire bonds are designated generally by reference numeral 42. There is thus provided the interconnections necessary to form a high density interconnected chip array which has pin out connections to the conductive patterns at the respective laminations of the multi-layer ceramic package.

With the high component density described, it is difficult to maintain the 10 mil spacing which is required for conductive patterns. This is achieved, in accordance with a feature of the present invention, in the manner illustrated in Figs. 2 and 3. As shown in these figures, the wire bonds converge upon the chip array connected at one end through a ball bond 44 (Fig. 5) to a chip 40 and at the other end through a wedge bond 46 to a conductive pattern on one or the other of the intermediate layer 14 or frame layer 18. In spite of the high density of LSI chip components and wire bonds, the 10 mil spacing of the conductive patterns is maintained by alternating between layers 14 and 18.

Obviously, there can be more than two alternating layers; three, four or even more layers for alternate wire bonding are contemplated. However, the basic concept, generally, is that by coupling the wire bonds between the centrally disposed high density chip array, and alternately differing levels of the metalized layers, it is possible to increase the number of wire bonds and thus achieve the desired centrally disposed component density while in no way compromising the necessary 10 mil spacing for the conductive patterns.

With regard to manufacture, the wire bonds between the central array and the conductive patterns at the various levels make appropriate connections from layer-to-layer as described, either through tunnels 32 or edge metalizations 34 (Figs. 3 and 4a) all of which ultimately lead to the base layer 12 and underlying pads 33 which are then bonded to appropriate locations on the underlying metalized board 24. The laminants may typically consist of aluminum silicate or other inert substrate materials, which, as stated previously, are green at the time the metalizations, tunnel and edge metalizations are formed thereon.

The layers having a conductive pattern, the ring 20, and the chip array, once the chip array is fixed and wire bondings made with the centrally disposed array, are surmounted with cover layer 22. The package as a whole is next fired (sealed) and the final product mounted on to the metalized board 24.

The chip array is mounted on the intermediate layer 14, and the chips 40 of the array are communicated chip-to-chip through lands 38 on the upper face of the intermediate layer 14, and other layers as required.

The chip array has wire bond connections 42 to the metalized ceramic conductor patterns, made by bonding the ends of the wire bonds so that adjacent wire bonds are connected from the chip array to alternating levels in the multi-layer ceramic package.

The package as a whole is next mounted on the metalized board 24 so that the pads 33 at the exterior surface of the package are mounted on various terminals of the metalized board having a predetermined printed circuit architecture and componentry.

It should be understood that any required conductive pattern can be screened on to the surface of the respective layers of the multi-layer ceramic package, and the conductive pattern as such, i.e. the particular architecture or pattern per se, for example as illustrated, does not form a part of the present invention.

It should be further emphasised that the 10 mil spacing is achievable in the present invention by reason of connecting first one wire from the chip array to a first level and then alternating the wire bonds to a second level, a third level, a fourth level, etc., thereby provid-

ing the means for maintaining a 10 mil of conductive patterns spacing in spite of the increased component density and the central converging of such wires. Quite obviously, if the 10 mil spacing is not maintained as an industry standard, it is equally possible to obtain an even higher component density with either an agreed upon less than 10 mil spacing and/or less than 10 mil bonding lands.

In all events, the present invention provides the possibility of maximum component density while maintaining a 10 mil spacing, but is equally applicable to whatever component density is desired, while achieving an inherently greater density for the respective wire bonds.

Although the present invention has been illustrated and described in connection with a single example embodiment, it will be understood that this is illustrative of the invention and is by no means restrictive thereof. For example, instead of three ceramic layers of the multi-layer ceramic package, it is possible to use four, five, or any number desired to achieve the desired combination of wire spacing, multi-layering, and various arrangements for the printed circuit network as well as the architecture of interconnected chip array. All of these changes are contemplated as part of the present invention and it is intended that such variations shall be included within the scope of the invention as defined by the following claims.

CLAIMS

1. A method for producing a high component density multi-layer chip carrier, comprising the steps of forming a first chip carrier layer adapted to receive at least one chip thereon, and at least one additional layer, forming pin-out conductive connections with said chip, forming metalized conductor paths on said respective layers, and forming wire connections from said chip alternating between staggered paths respectively formed on the different levels of said layers.

2. The method in accordance with claim 1, including the steps of forming said multi-layers of individually compacted ceramic particles, and simultaneously firing said compacted ceramic layers to sinter the particles and to bond the respective layers together.

3. The method in accordance with claim 1 or claim 2, including the step of disposing a ring and cover at the upper end of said multi-layers, and providing a plurality of pads at the outer face of said multi-layer carrier and adapted to serve as outlets on a metalized board.

4. The method in accordance with claim 1 or claim 2 or claim 3, including the steps of forming a plurality of lands on the layer adapted for receiving chips and effecting short wire bonding between respective chips through said lands.

5. The method in accordance with any of claims 1 to 4, including the step of sealing an interior cavity of said carrier which receives said chip and wherein said chip is mounted.

6. The method in accordance with any of claims 1 to 5, including the step of disposing said wire connections between the chip and the metalized paths of said layers in alternating multi-level connections between said chip and layers to not less than two alternating layers of said multi-layer chip carrier.

7. A multi-layer ceramic package, comprising a plurality of spaced apart laminants including an intermediate level laminant adapted to receive a chip array, at least one chip disposed on said intermediate level laminant, conductive patterns on respective ones of said laminants, selected ones of said conductive patterns having wire bonds, metalized conductive means interconnecting the conductive patterns on the respective multi-layered laminants, and wire connections maintaining not less than a predetermined spacing of said wire bonds respectively by extending between said chip at one end and to alternating levels of laminants at the other end to provide electrical connections from the chip to said conductive patterns.

8. A multi-layer ceramic package in accordance with claim 7, wherein said predetermined spacing is 10 mil.

9. The multi-layer ceramic package in accordance with claim 7 or claim 8, wherein the conductive means comprises metalized-filled openings forming conductive paths between the conductive patterns on respective sides of selective ones of the laminants forming the ceramic package, and edge-formed metalized conductive paths interconnecting the conductive patterns on other of the multi-layer ceramic laminants, whereby composite conductive patterns of said laminants are connected together and to said chip.

10. The multi-layer ceramic package in accordance with any of claims 7 to 9, including means forming lands at the level of the ceramic package wherein a chip array is disposed, and short wire bond connections to the land providing a conductor network between the chips of the chip array, said multi-layer ceramic package being adapted for high component density.

11. The multi-layer ceramic package in accordance with any of claims 7 to 10, including means forming an internal cavity of said package, the intermediate level laminant includes internal cavity lands for electrically inter-connecting the chip.

12. The multi-layer ceramic package in accordance with any of claims 7 to 11, wherein said laminants are formed as compacted ceramic particle layers, and subsequently fired to develop bonded inter-layer connections between confronting surfaces of the respective ceramic laminants.

13. The multi-layer ceramic package in accordance with any of claims 7 to 12, including a high component density chip array, an internal cavity for receiving said high component density chip array, means forming an interconnected relation of said chips and wire bonds from said interconnected chip array to alternating levels of conductive patterns on the respective multi-level ceramic lamihants to form a multi-layer ceramic framing for said multi-layer ceramic package.

14. A method of producing a multi-layer chip carrier substantially as hereinbefore described with reference to the accompanying drawings.

15. A multi-layer ceramic package substantially as hereinbefore described with reference to the accompanying drawings.

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